

IN THE CLAIMS

Claims 1-30 (Canceled).

Claim 31 (New): A nonvolatile semiconductor device comprising:

at least one memory cell;

a bit line connected to the memory cell; and

a bit line control circuit including a capacitor, a MOS transistor, a flip-flop circuit, a first transfer gate connected between the capacitor and the bit line, a second transfer gate between the capacitor and the flip-flop circuit, and a third transfer gate connected between the flip-flop circuit and a gate electrode of the MOS transistor, wherein a source electrode of the MOS transistor is coupled to the capacitor, a drain electrode of the MOS transistor is coupled to a voltage source, and the MOS transistor selectively changes an amount of charges stored in the capacitor according to a voltage level of the gate electrode selectively boosted by a change of the voltage source.

Claim 32 (New): The device according to claim 31, further comprising:

a fourth transfer gate connected between the source electrode of the MOS transistor and the capacitor, and

the bit line during a program of the memory cell having one of three potential levels controlled by the flip-flop circuit and the voltage level of the gate electrode of the MOS transistor.

Claim 33 (New): The device according to claim 31, wherein each of the first, second and third transfer gates and the MOS transistor is an N-type MOS transistor.

Claim 34 (New): The device according to claim 32, wherein the fourth transfer gate is an N-type MOS transistor.

Claim 35 (New): The device according to claim 31, wherein data stored in the flip-flop circuit is transferred to the gate electrode of the MOS transistor before the flip-flop circuit senses and stores data on the capacitor.

Claim 36 (New): The device according to claim 31, wherein the memory cell comprises a charge accumulation layer.

Claim 37 (New): The device according to claim 36, wherein the charge accumulation layer is controlled by a control gate of the memory cell.

Claim 38 (New): The device according to claim 31, further comprising:
plural memory cells; and
a NAND cell unit connected in series with the plural memory cells.

Claim 39 (New): A nonvolatile semiconductor device comprising:
at least one memory cell;
a bit line connected to the memory cell; and
a bit line control circuit including a capacitor, a MOS transistor, a flip-flop circuit, a first transfer gate connected between the capacitor and the bit line, a second transfer gate between the capacitor and the flip-flop circuit, a third transfer gate connected between the flip-flop circuit and a gate electrode of the MOS transistor, and a fourth transfer gate connected between a source electrode of the MOS transistor and the capacitor, wherein the

bit line during a program of the memory cell has one of three potential levels controlled by the flip-flop circuit and the voltage level of the gate electrode.

Claim 40 (New): The device according to claim 39, wherein a drain electrode of the MOS transistor is coupled to a voltage source (VREG), and the MOS transistor selectively changes an amount of charges stored in the capacitor according to a voltage level of the gate electrode selectively boosted by a change of the voltage source.

Claim 41 (New): The device according to claim 39, wherein each of the first, second, third and fourth transfer gates and the MOS transistor is an N-type MOS transistor.

Claim 42 (New): The device according to claim 39, wherein data stored in the flip-flop circuit is transferred to the gate electrode of the MOS transistor before the flip-flop circuit senses and stores data on the capacitor.

Claim 43 (New): The device according to claim 39, wherein the memory cell comprises a charge accumulation layer.

Claim 44 (New): The device according to claim 43, wherein the memory cell includes a control gate and the charge accumulation layer is controlled by the control gate of the memory cell.

Claim 45 (New): The device according to claim 39, further comprising:
plural memory cells; and
a NAND cell unit connected in series with the plural memory cells.